REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The examiner rejects Claims 1-13 and 15-16 under 35 U.S.C. § 102(b) as being anticipated by Papaliolios. The examiner states that Fig. 5 shows a power efficiency control circuit comprising a plurality of multiplexers having a common input node 505.

This rejection is respectfully traversed. The circuit shown in Fig. 5 of Papaliolios has dual inputs 505, 550 to the circuit which drives the output transistors 545 and 590. The examiner is taking the signal 505 which passes through inverter 510, the output of which is coupled to switching the control inputs to the multiplexers 530, 570 which is not an input signal to control the output transistors, as it is in the present invention. This can be clearly seen by looking at the two input signals 810, 820 in Fig. 8 of the Papaliolios patent. As can be clearly seen, the two signals are not alike, so there is no single input signal for controlling the two output transistors, as in the present invention. The result is clearly shown in Fig. 7 of the reference. The first spike of current 310 is eliminated because the input signal driving the MUX comes off the output pull-up driver 505. However, the second current spike 730 is delayed and only diminished by about 20% because the output control signal is being controlled by the signal on line 550 whereas the multiplexers are controlled by the input on line 505 through inverter 510. Thus, the utilization of the time delays in the inverters in the cited reference does not produce the same result as the present invention in which both current spikes are substantially eliminated, as clearly shown in Fig. 6 of the present application. The claims have been amended in order to clarify this for the examiner.

Accordingly, Applicants believe that the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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